WHAT IS CLAIMED IS:

1. A random access memory comprising:

a plurality of data pads;

an array of memory cells comprising a first portion of memory cells and a second portion of memory cells;

a first line configured to receive first data signals between the first portion of memory cells and the data pads; and

a second line configured to receive second data signals between the second portion of memory cells and the data pads, wherein the first portion of memory cells is configured to be made inaccessible to eliminate the first data signals and a first number of the data pads and the second portion of memory cells is configured to be made inaccessible to eliminate the second data signals and a second number of the data pads.

2. The random access memory of claim 1, wherein the first number of the data pads is equal to the second number of the data pads.

3. The random access memory of claim 1, wherein the first portion of memory cells is separate from the second portion of memory cells.

4. The random access memory of claim 1, wherein the first portion of memory cells and the second portion of memory cells have the same number of accessible memory cells.

5. The random access memory of claim 1, wherein the first line comprises a first data bus that receives eight first data signals and the second line comprises a second data bus that receives eight second data signals.

6. The random access memory of claim 1, further comprising:

word lines extending along rows of the array of memory cells; and

bit lines extending along columns of the array of memory cells, wherein a memory cell is located at each cross point of one of the word lines and one of the bit lines.

7. The random access memory of claim 6, wherein a first portion of the bit lines is electrically coupled to the first line and a second portion of the bit lines is electrically coupled to the second line.

8. The random access memory of claim 1, wherein the first portion of memory cells stores even data and odd data and the second portion of memory cells stores even data and odd data.

9. The random access memory of claim 1, wherein the memory has a page length of 16k bits.

10. The random access memory of claim 1, wherein the memory has a page length of 8k bits.

11. The random access memory of claim 1, wherein the first line comprises a fuse to be blown to deactivate the first portion of memory cells and the second line comprises a fuse to be blown to deactivate the second portion of memory cells.

12. The random access memory of claim 1, comprising a multiplexer configured to select the first data signals and the second data signals and provide the selected signals to the data pads.

13. A random access memory comprising:

an array of memory cells;

first lines crossing the array of memory cells and configured to select rows of memory cells in the array of memory cells; and

second lines crossing the first lines at memory cells in the array of memory cells and configured to select columns of memory cells in the array of memory cells, wherein the selected columns of memory cells communicate with data pads and the array of memory cells is configured to be reduced to eliminate a number of the selected columns of memory cells that communicate with the data pads.

14. The random access memory of claim 13, wherein each of the second lines comprises a fuse to be blown to reduce the array of memory cells.

15. The random access memory of claim 13, wherein the array of memory cells is configured to be reduced with a first cut option to one half of the array of memory cells and with a second cut option to the other half of the array of memory cells.

16. The random access memory of claim 13, wherein the array of memory cells is configured to be reduced to one half of the array of memory cells with a first cut option and the other half of the array of memory cells with a second cut option, wherein the one half of the array of memory cells stores even data and odd data and the other half of the array of memory cells stores even data and odd data.

17. The random access memory of claim 13, comprising a multiplexer configured to select data signals from the second lines and provide the selected data signals to the data pads.

18. A random access memory comprising:

banks of addressable memory cells;

data pads configured to receive data signals;

means for communicating the data signals between the banks and the data pads; and

means for reducing the data pads and the addressable memory cells.

19. The random access memory of claim 18, wherein the means for reducing comprises means for reducing the data pads by one half.

20. The random access memory of claim 18, wherein the means for reducing comprises means for reducing the addressable memory cells by one half.

21. The random access memory of claim 18, wherein the means for reducing comprises means for providing a first cut option and a second cut option and the means for communicating comprises a multiplexer configured to select the data signals based on the first cut option and the second cut option to communicate the data signals between the banks and the data pads.

22. The random access memory of claim 18, wherein the means for reducing comprises fuses in the means for communicating.

23. A method for reducing storage capacity in a random access memory, comprising:

preventing access to portions of the random access memory; and

eliminating data pads electrically coupled to the portions of the random access memory where access is prevented.

24. The method of claim 23, wherein preventing access comprises blowing fuses on data lines electrically coupled to the data pads.

25. The method of claim 23, wherein eliminating data pads comprises reducing the data pads from 16 data pads to 8 data pads.

26. The method of claim 23, wherein eliminating data pads comprises reducing the data pads from 8 data pads to 4 data pads.

27. The method of claim 23, wherein preventing access reduces a page length of the random access memory from 16k bits to 8k bits.

28. The method of claim 23, wherein preventing access reduces addressable memory in the random access memory from 512M bits to 256M bits.

29. A random access memory comprising:

a plurality of data pads comprising a first portion of data pads and a second portion of data pads;

an array of memory cells comprising a first portion of memory cells and a second portion of memory cells;

a plurality of word lines extending along rows of the array of memory cells; and

a plurality of bit lines extending along columns of the array of memory cells comprising a first portion of bit lines and a second portion of bit lines;

wherein a memory cell is located at each cross point of one of the word lines and one of the bit lines, the first portion of data pads is electrically coupled to the first portion of memory cells through the first portion of bit lines and the second portion of data pads is electrically coupled to the second portion of memory cells through the second portion of bit lines, the first portion of memory cells is configured to be made inaccessible by decoupling the first portion of data pads from the first portion of memory cells, and the second portion of memory cells is configured to be made inaccessible by decoupling the second portion of data pads from the second portion of memory cells.

30. The random access memory of claim 29, wherein the bit lines comprise fuses for decoupling the first portion of data pads from the first portion of memory cells and the second portion of data pads from the second portion of memory cells.

31. The random access memory of claim 29, comprising a multiplexer electrically coupled to the first and second portions of bit lines and the first and

second portions of data pads, the multiplexer configured to selectively couple the first and second portions of bit lines to the first and second portions of data pads.

32. The random access memory of claim 29, wherein one half of the first portion of memory cells stores even data and the other half of the first portion of memory cells stores odd data and one half of the second portion of memory cells stores even data and the other half of the second portion of memory cells stores odd data.

33. A dynamic random access memory comprising:

a plurality of data pads;

an array of memory cells comprising a first portion of memory cells and a second portion of memory cells;

a first line configured to receive first data signals between the first portion of memory cells and the data pads; and

a second line configured to receive second data signals between the second portion of memory cells and the data pads, wherein the first portion of memory cells is configured to be made inaccessible to eliminate the first data signals and a first number of the data pads and the second portion of memory cells is configured to be made inaccessible to eliminate the second data signals and a second number of the data pads.

34. The dynamic random access memory of claim 33, wherein the dynamic random access memory is a synchronous dynamic random access memory.

35. The dynamic random access memory of claim 33, wherein the dynamic random access memory is a double data rate synchronous dynamic random access memory.